IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Zahid ANSARI et al.

Application No.: 09/937,680

Filing Date: November 29, 2001

For: METHOD AND APPARATUS FOR PROVIDING PULSE WIDTH MODULATION

Confirmation No.: 3828

Patent No.: 6,867,645 B1

Patent Date: March 15, 2005

Attorney Docket No.: 81400-4000

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.323

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The corrections are listed on the attached Form PTO-1050. The corrections requested are as follows:

Drawings:

On the title page and in FIG. 1, in the power supply 102, delete the upper "–" sign and insert -- + --.

On the title page and in FIG. 3, in the power supply 102, delete the upper "–" sign and insert -- + --; and to the left of the "LOAD" box, delete the "–" sign and insert -- + --.

FIG. 9, at the "Vdc" location, delete the upper "–" sign and insert -- + --.

Column 3:

Line 8, after "apparatuses for practicing the invention are" delete "ill ated." and insert -- illustrated. --

Line 61, after "The inverter circuit is preferably an" delete "II-bridge" and insert -- H-bridge --.

Column 4:

Line 10, after "port" delete "**108**" and insert -- **109** --.

Column 5:

Line 32, before "FIG. 3." delete "LEI".

A marked-up copy of the patent showing the requested changes is enclosed. The changes are to correct errors of a clerical or typographical nature and do not involve changes that would constitute new matter or require reexamination.

A fee of $100 is believed to be due for this request. Please charge the required fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

3-6-07

Date

Allan A. Fanucci, Reg. No. 30,256

WINSTON & STRAWN LLP
Customer No. 28765

212-294-3311

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.: 6,867,645 B1
APPLICATION NO.: 09/937,680
DATED: March 15, 2005
INVENTOR(S): Ansari et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Drawings:
On the title page and in FIG. 1, in the power supply 102, delete the upper "–" sign and insert -- + --.
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US006867645B1

(12) **United States Patent**
Ansari et al.

(10) **Patent No.: US 6,867,645 B1**
(45) **Date of Patent: Mar. 15, 2005**

(54) **METHOD AND APPARATUS FOR PROVIDING PULSE WIDTH MODULATION**

(75) Inventors: **Zahid Ansari**, Menlo Park, CA (US); **Bruce L. Prickett**, Fremont, CA (US); **Jonathan Andrew Guy**, Austin, TX (US)

(73) Assignee: **Daydreams LLC**, West Palm Beach, FL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/937,680**

(22) PCT Filed: **Mar. 28, 2000**

(86) PCT No.: **PCT/US00/08562**

§ 371 (c)(1),
(2), (4) Date: **Nov. 29, 2001**

(87) PCT Pub. No.: **WO00/59114**

PCT Pub. Date: **Oct. 5, 2000**

Related U.S. Application Data

(60) Provisional application No. 60/164,326, filed on Nov. 7, 1999, provisional application No. 60/163,707, filed on Nov. 5, 1999, provisional application No. 60/164,083, filed on Nov. 5, 1999, and provisional application No. 60/126,770, filed on Mar. 29, 1999.

(51) **Int. Cl.**[7] **H02M 7/162**

(52) **U.S. Cl.** **327/588**; 327/423; 363/132

(58) **Field of Search** 327/587–588, 327/423, 494, 110; 363/132–133; 332/109

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,325,112	A *	4/1982	Otsuka	363/42
5,021,936	A *	6/1991	Nishizawa et al.	363/41
5,373,195	A	12/1994	De Doncker et al.	307/45
5,589,805	A	12/1996	Zuraski et al.	322/109
5,710,699	A	1/1998	King et al.	363/132
5,767,740	A	6/1998	Fogg	310/10
6,005,316	A	12/1999	Harris	310/90.5
6,031,738	A	2/2000	Lipo et al.	363/37

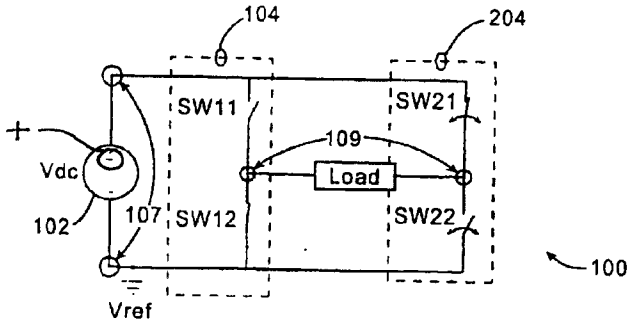
* cited by examiner

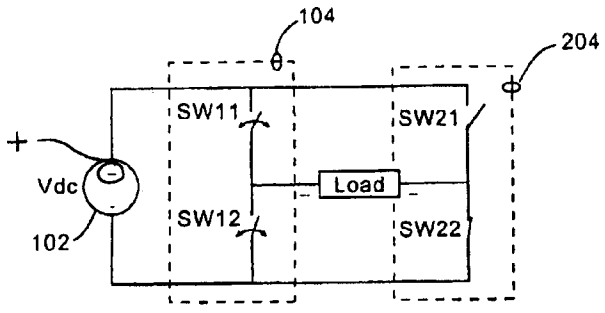
Primary Examiner—Quan Tra
(74) *Attorney, Agent, or Firm*—Winston & Strawn LLP

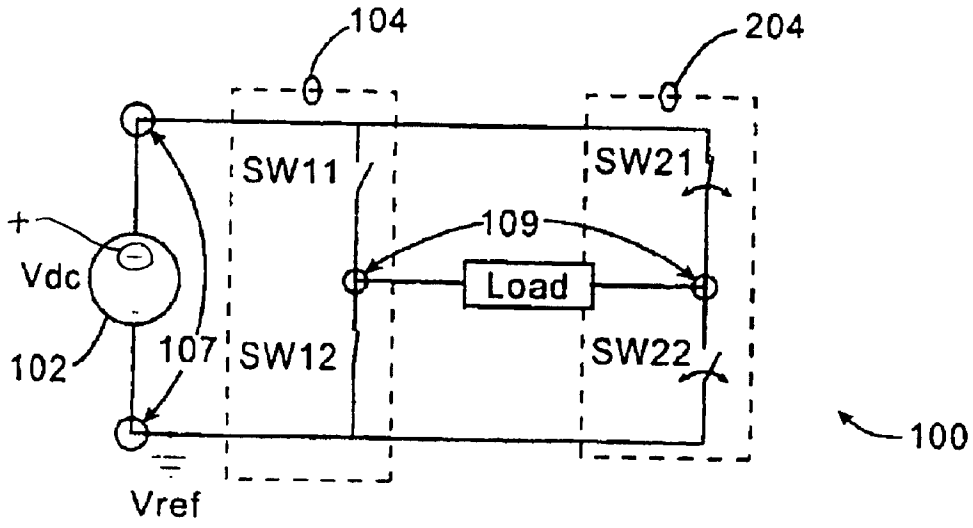
(57) **ABSTRACT**

A pulse width modulation scheme allows the creation of a unipolar pulse width modulated output signal. Two switching circuits (**104, 204**), preferably different legs of an inverter circuit, can operate to not only modulate an input voltage but also to reverse the polarity of the PWM output signal. Both switching circuits can be configured to accomplish both features, thus the switching load is spread out across all four switches.

8 Claims, 7 Drawing Sheets



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204
SW11
SW21
+
Vdc
109
Load
102
107
SW12
SW22
100
Vref

FIG. 1

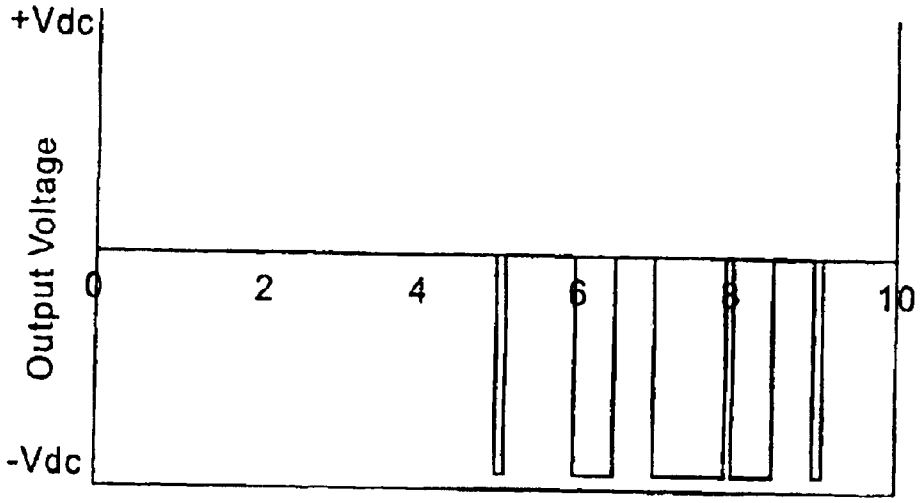
+Vdc
Output Voltage
0
2
4
6
8
10
-Vdc

FIG. 2

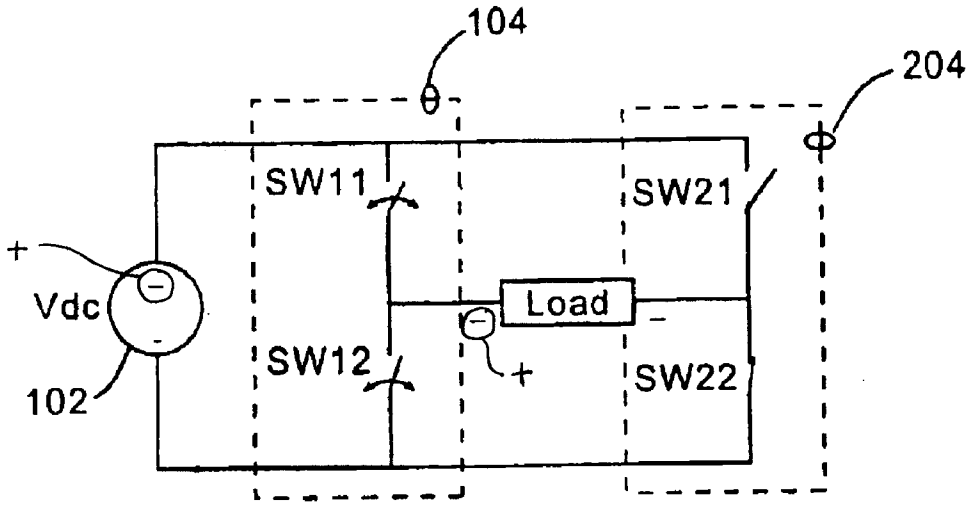
104
204
SW11
SW21
+
Vdc
-
Load
-
SW12
+
SW22
102

FIG. 3

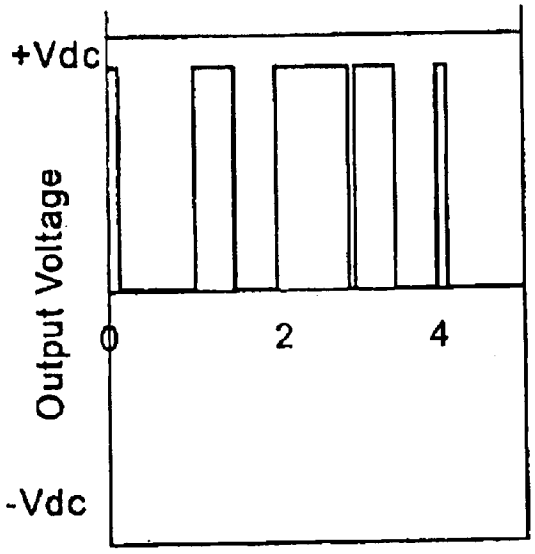
+Vdc
Output Voltage
0
2
4
-Vdc

FIG. 4

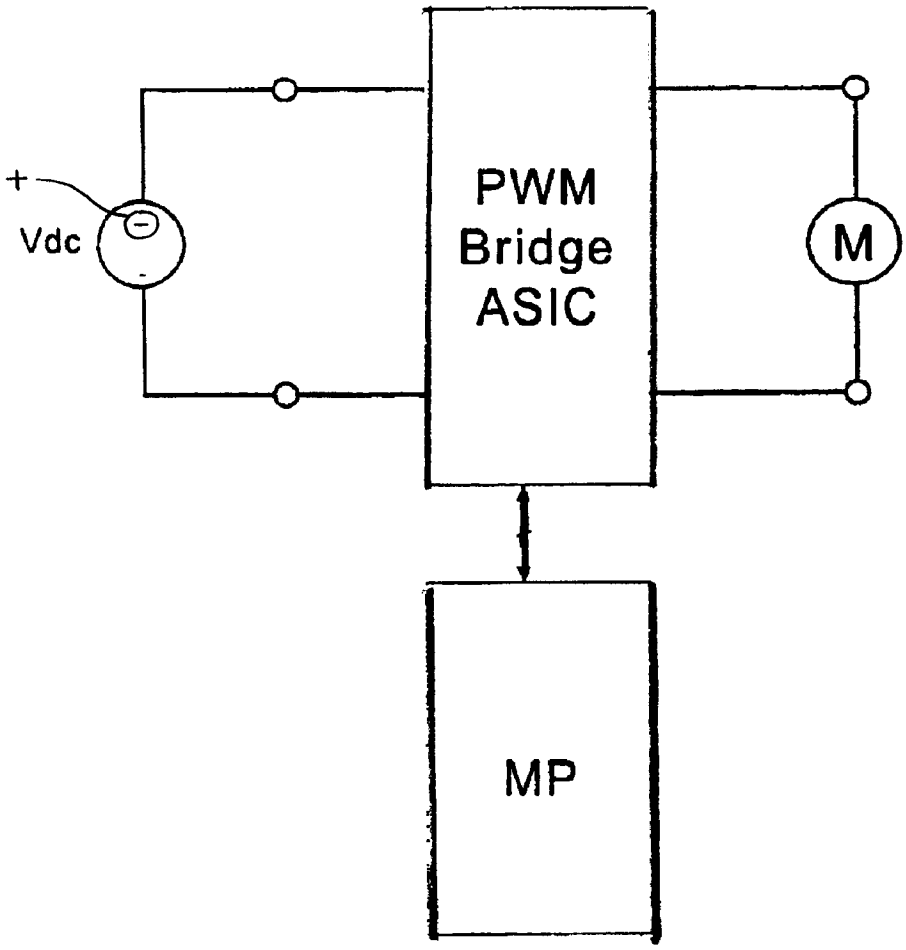

FIG. 9

load during operation. The second switching circuit may be used in a similar fashion so as to reverse polarity at the output and to provide a negative PWM signal at the output.

Other and further advantages and features of the invention will be apparent to those skilled in the art from a consideration of the following description taken in conjunction with the accompanying drawings wherein certain methods and apparatuses for practicing the invention are illustrated. However, it is to be understood that the invention is not limited to the details disclosed but includes all such variations and modifications as fall within the spirit of the invention and the scope of the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a circuit in which a switching circuit modulates an input signal to determine pulse width and spacing of pulses while a second switching circuit controls the polarity of the output signal.

FIG. **2** shows the output signal produced by the circuit in FIG. **1**.

FIG. **3** shows the configuration of the circuit in FIG. **1** in which the second switching circuit controls the polarity of the output signal while the first switching circuit modulates the input signal to determine pulse width and spacing of pulses.

FIG. **4** shows the output signal produced by the circuit in FIG. **3**.

FIG. **5** shows a portion of a pulse width modulation output signal with a superimposed equivalent sine wave that corresponds to the PWM output signal.

FIG. **6** shows a conventional bipolar pulse width modulation output signal.

FIG. **7** shows a circuit configuration used to produce the output signal shown in FIG. **6**, wherein a set of switches that operates as a conducting pair and as a non-conducting pair is shown within a dashed border.

FIG. **8** shows a configuration of the circuit in FIG. **7** wherein the remaining set of switches that operates as a conducting pair and as a non-conducting pair is shown within a dashed border.

FIG. **9** shows an embodiment in which a processor provides control signals to an application specific integrated circuit bridge to produce a pulse width modulated output signal that powers a motor.

FIG. **10** shows a flow diagram that illustrates the method of operation of producing a pulse width modulated output voltage.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Referring now to FIG. **1**, an embodiment of the invention can be seen as circuit **100**. An inverter circuit is shown having four switches (SW**11**, SW**12**, SW**21**, and SW**22**). A power supply **102** provides an input voltage to the inverter through an input **107**. In addition, an output is established between the switches of the inverters to electrically couple an output signal to the load.

The inverter circuit is preferably an H-bridge inverter circuit comprised of power transistors, such as MOSFET's. Alternatively, other power switching devices could be utilized as well. For example for motor loads of several hundred horsepower, IGBT's may be used or GTO's could be used for motors of several thousand horsepower. The inverter is preferably comprised of two switching circuits. A second switching circuit **204** is comprised of a first switch (SW**21**) and a second switch (SW**22**) electrically connected in series. Similarly, a first switching circuit of the inverter circuit is comprised of a first switch (SW**11**) and a second switch (SW**12**) electrically connected in series. Preferably, these two switching circuits are connected in parallel. Also, it is preferred that the two switching circuits be electrically coupled in parallel with an input **107** which is shown connected in parallel with the DC voltage source. An output port **108** is preferably established between the two switching circuits **104** and **204**. One of the terminals of the input can be grounded so as to establish a reference voltage (Vref) of zero volts. Nevertheless, an offset could also be introduced into the circuit to produce a biased pulse width modulated (PWM) output signal.

Preferably, the input voltage source **102** is a DC voltage source that produces a DC voltage signal for manipulation by the H-bridge inverter circuit. While the phrase DC voltage is used throughout the specification and claims, it should be understood that a pure DC voltage is not required. As those of ordinary skill in the art would understand, practical circuits introduce a ripple into a voltage. So, those voltage signals are intended to be included under the definition of a DC voltage, as well.

The circuit of FIG. 1 is utilized to produce the output waveform shown in FIG. **2**. Often, this waveform is referred to as a partial unipolar pulse width modulated waveform. FIG. **2** shows a series of pulses of varying width, but of common voltage magnitude, namely −Vdc. The polarity of the signal in FIG. **2**, i.e., negative Vdc instead of positive Vdc, is determined by the configuration of the first switching circuit **104**. Switch SW**12** is shown in a conducting state; thus, it provides a path for a negative DC voltage signal to be applied to the load. The DC voltage signal output across the load will necessarily be −Vdc or zero volts in this configuration. Thus, switches SW**11** and SW**12** control the polarity when maintained in opposite conducting and non-conducting states. Thus, in the circuit of FIG. **1**, the switching circuit **204** actually reverses the voltage of the input voltage +Vdc so that a negative PWM output voltage signal is created, oscillating between −Vdc and 0 volts.

Switching circuit **204** in FIG. **1** determines the pulse width and pulse intervals, that is to say, it modulates the input signal to produce the output waveform. FIG. **1** shows switches SW**21** and SW**22** with double headed arrows. This is to indicate that these switches oscillate between conducting and non-conducting states. Preferably, the two switches are not in conducting states simultaneously. Also, it is preferred that when one of these switches is switched from its conducting state to its non-conducting state that the other switch enter its conducting state from its non-conducting state. Thus, it is preferred to keep these switches in opposite states of conduction when modulating the DC signal.

The width and spacing of the PWM output signal pulses are determined by one of the various PWM schemes. Examples of such schemes are shown, for example, in: "Power Electronics" by Mohan, Undeland, and Robbins, Second Edition, John Wiley and Sons, Inc., 1995, which is hereby incorporated by reference for all that it discloses and for all purposes; "A Centroid-Based PWM Switching Technique for Full-Bridge Inverter Applications" by Ali Yazdian-Varjani et al., in IEEE Transactions on Power Electronics, Vol. 13 No. 1, January 1998, which is hereby incorporated by reference for all that it discloses and for all purposes; "electrical Machines, Drives, and Power Systems, Fourth Edition," by Theodore Wildi, Prentice Hall, 2000, which is hereby incorporated by reference for all that it discloses and

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Switching circuit **204** in FIG. **1** determines the pulse width and pulse intervals, that is to say, it modulates the input signal to produce the output waveform. FIG. **1** shows switches SW**21** and SW**22** with double headed arrows. This is to indicate that these switches oscillate between conducting and non-conducting states. Preferably, the two switches are not in conducting states simultaneously. Also, it is preferred that when one of these switches is switched from its conducting state to its non-conducting state that the other switch enter its conducting state from its non-conducting state. Thus, it is preferred to keep these switches in opposite states of conduction when modulating the DC signal.

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for all purposes. In addition, U.S. Provisional Applications 60/126,770 filed on Mar. 29, 1999, 60/164,083 filed Nov. 5, 1999, 60/163,707 filed Nov. 5, 1999, 60/164,326 filed Nov. 7, 1999 are hereby incorporated by reference in their entirety for all that they disclose and for all purposes. These schemes would be readily understood by one of ordinary skill in the art. Thus, depending on the PWM scheme selected, control signals can be generated and transmitted by a processor to the inverter bridge circuit to control the timing of the operation of the switches. Thus, the opening and closing of switches SW21 and SW22 in FIG. 1 produces the pulses and pulse spacing in FIG. 2. Namely, switch SW22 is placed in the conducting state and switch SW21 is placed in a non-conducting state when a zero voltage is needed. Alternatively, switch SW22 is placed in a non-conducting state and switch SW21 is placed in a conducting state when a negative voltage is required to be output.

FIG. 3 shows the circuit of FIG. 1 configured to produce a positive portion of the unipolar PWM output voltage signal. In FIG. 3, switching circuit **204** is placed in the static arrangement where switch SW22 is maintained in a conducting state while switch SW21 is maintained in a non-conducting state. Thus switching circuit **204** is operable to control the polarity of the output signal.

In FIG. 3, switching circuit **104** is operable to modulate the input voltage Vdc so as to control the pulse width and pulse spacing of the output voltage pulses. Switches SW11 and SW12 operate in the same fashion as switches SW21 and SW22 operated to produce the negative PWM output waveform. Thus, as can be seen in FIG. 4, a positive portion of the unipolar PWM waveform is generated by the circuit shown in FIG. 3.

By combining the switch arrangements of FIG. 1 and FIG. 3, a unipolar pulse width modulated output waveform is generated, as illustrated in FIG. 5. FIG. 5 also shows a sine wave having a fundamental period (T). This sine wave represents the equivalent sine wave that, in the case of an induction motor load, would cause the induction motor to run at the same speed as that caused by the unipolar pulse width modulated waveform of FIG. 5. While the frequency of this equivalent waveform, i.e., the sine wave, is referred to as the fundamental frequency, the frequency of the PWM waveform is referred to as the carrier frequency. Thus, the circuit of FIG. 1 is utilized to produce a negative portion of the unipolar pulse width modulated waveform relative to the reference voltage for approximately one half of the fundamental period. Similarly, the circuit of FIG. 3 is utilized to produce the positive portion of the unipolar pulse width modulated waveform relative to the reference voltage for approximately the other half of the fundamental period. The switching arrangement can be repeated indefinitely for additional periods

FIG. 6 illustrates the output voltage produced by conventional systems known as bipolar pulse width modulated voltage signal. As can be seen, the transition of this type of waveform results in a transition of 2 Vdc. Thus, as those of ordinary skill in the art would appreciate, the voltage overshoot is twice the magnitude of the transition, namely 4 Vdc. In contrast, the unipolar PWM scheme outlined above, would only produce a transition of Vdc and an associated overshoot of 2 Vdc across the switch. Thus, the unipolar scheme is much less damaging to the components of the load, because less voltage is placed across it.

FIGS. 7 and 8 highlight the association of switches used in the conventional bipolar PWM scheme. As can be seen in FIG. 7 and FIG. 8, switches SW11 and SW22 operate in unison, while switches SW12 and SW21 also operate in unison. Thus, when SW11 and SW22 are in a conducting state and SW12 and SW21 are in a non-conducting state, a voltage of +Vdc is applied across the load. Similarly, when SW12 and SW21 are in a conducting state and SW11 and SW22 are in a non-conducting state, as shown in FIG. 8, then a voltage of -Vdc is applied across the load. Consequently, in order for a transition of the PWM output signal to occur, all four switches must change state. This creates heat, electrical noise, and shortens the life span of the switches. In contrast, the circuits of FIGS. 1 and 3 generally only require a transition of two switches in order to cause a transition of the output signal (although 4 additional switch transitions could be required each cycle to account for the two polarity changes each cycle). Thus, the disclosed unipolar PWM switching scheme is accomplished with fewer switch transitions than that required to produce a bipolar pulse width modulated output voltage.

Similarly, in contrast to the unipolar PWM scheme disclosed by Yazdian-Varjani et al., as referenced above, the present unipolar PWM scheme spreads the switching evenly across the four switches of the inverter. In the method of Yazdian-Varjani et al., a single switching circuit was responsible for modulating the DC input signal, while the other switching circuit was solely responsible for controlling the polarity of the output PWM signal. The PWM scheme disclosed herein distributes those responsibilities to both switching circuits. Thus, each switching circuit can be operated to control polarity as well as to modulate the DC voltage signal. Thus, it is advantageous in that it spreads the switching load across all of the switches (SW11, SW12, SW21, and SW22). It also provides symmetry of the two half-bridges. Thus, timing of transitions is simplified because response time of the switches would be similar, as opposed to the system of Yazdian-Varjani et al. in which different switches were proposed for the different half bridges.

The preferred embodiment of the invention has been described with the high side switches (i.e., switches SW11 and SW21 which are electrically coupled to the high side of the power supply) operated so as not to be in a conducting state for a half-cycle of the fundamental output frequency. Rather, as noted in FIG. 1 and FIG. 3, the low side switches (SW12 and SW22) are used to control the polarity by remaining on for approximately one half of the fundamental output period. This is yet another advantage over the scheme proposed by Yazdian-Varjani et al. because it typically requires less complicated circuitry to keep the low side switches in a conducting state as compared to the high side switches. For example, a lower cost "boot strap supply" can be used for the high side FET gate drivers in this preferred embodiment. Nevertheless, it should be understood that one might choose to reverse the conduction states of switches SW11 and SW12 in FIG. 1 and SW21 and SW22 in FIG. 3. Thus, such an alternative embodiment would also be covered by this invention.

FIG. 9 shows an embodiment in which the inverter bridge circuit is configured as part of an application specific integrated circuit, as would be understood by a person of ordinary skill in the art. The ASIC may either house just the power transistors, or it may be configured with a microprocessor so as to allow the control signals for the switches to be routed directly to the power transistors without any external wiring. In FIG. 9, a microprocessor is shown separate from the ASIC. Similarly, the ASIC could also include a power supply or power conversion circuit to produce the DC waveform utilized in creating a pulse width modulated output.